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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,316	02/08/2002	Junichi Karasawa	81751.0029	9698
26021	7590	07/08/2004	EXAMINER	
HOGAN & HARTSON L.L.P. 500 S. GRAND AVENUE SUITE 1900 LOS ANGELES, CA 90071-2611				LOKE, STEVEN HO YIN
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/072,316	KARASAWA ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Steven Loke	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 11 May 2004.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-15, 17 and 18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-12, 17 and 18 is/are rejected.
- 7) Claim(s) 13-15 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All
  - b) Some \*
  - c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-12, 17 and 18 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Komori.

In regards to claim 1, Komori shows all the elements of the claimed invention in figs. 39-41. It is a semiconductor device provided with a memory cell including a first driver transistor [101], a second driver transistor [104], a first transfer transistor [103], a second transfer transistor [106], a first load transistor [102] and a second load transistor [105]. The semiconductor transistor comprising: a first gate-gate electrode layer [111] including a gate electrode of the first load transistor [102] and a gate electrode of the first driver transistor [101]; a second gate-gate electrode layer [112] including a gate electrode of the second load transistor [105] and a gate electrode of the second driver transistor [104]; a first drain-drain wiring layer [116] which forms a part of a connection layer that electrically connects a drain region of the first load transistor [102] and a drain region of the first driver transistor [101]; a second drain-drain wiring layer [115] which forms a part of a connection layer that electrically connects a drain region of the second load transistor [105] and a drain region of the second driver transistor [104]; a first drain-gate wiring layer [111] which forms a part of a connection layer that electrically connects

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the first gate-gate electrode layer [111] and the second drain-drain wiring layer [115]; a second drain-gate wiring layer [116] which forms a part of a connection layer that electrically connects the second gate-gate electrode layer [112] and the first drain-drain wiring layer [116]; and a first active region [140] in which the first load transistor [102] is provided, wherein the first drain-gate wiring layer [111] and the second drain-gate wiring layer [116] are located in different layer levels, respectively (fig. 41), and wherein a first protruded active region is provided in a manner to protrude from an end portion of the first active region.

In regards to claim 2, Komori further discloses the first protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors [101, 104] are provided.

In regards to claim 3, Komori further discloses a part of the first active region [140] and the first protruded active region form an L-shape.

In regards to claim 4, Komori further discloses a second active region [160] in which the second load transistor [105] is provided; and a second protruded active region provided in a manner to protrude from an end portion of the second active region.

In regards to claim 5, Komori further discloses the second protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors [101, 104] are provided.

In regards to claim 6, Komori further discloses a part of the second active region and the second protruded active region form an L-shape.

In regards to claim 7, Komori further discloses the first drain-gate wiring layer [111] is electrically connected to the second drain-drain wiring layer [115] through a contact section [222], wherein the second drain-gate wiring layer [116] is electrically connected to the second gate-gate electrode layer [112] through a contact section [310], and electrically connected to the first drain-drain wiring layer [116] through a contact section (the contact surface between the horizontal portion of layer [116] and the vertical portion of layer [116] in fig. 40).

In regards to claim 8, Komori further discloses the first drain-gate wiring layer [111] is located in a layer lower than the second drain-gate wiring layer [116].

In regards to claim 9, Komori further discloses the first drain-gate wiring layer [111] is located in a layer in which the first gate-gate electrode layer [111] is provided.

In regards to claim 10, Komori further discloses the second drain-gate wiring layer [116] is formed across a plurality of layers [111, 115].

In regards to claim 11, Komori further discloses the second drain-gate wiring layer [116] includes a lower layer (the layer formed in the contact hole [310]) of the second drain-gate wiring layer and an upper layer [116] of the second drain-gate wiring layer, and wherein the upper layer is located in a layer over the lower layer, and electrically connected to the lower layer.

In regards to claim 12, Komori further discloses the upper layer is electrically connected to the lower layer through a contact section (the contact surface between the layer [116] and the layer formed in the contact hole [310]).

In regards to claim 17, Komori further discloses a memory system (SRAMs) provided with the semiconductor device defined in any of claims 1-12 (col. 1, line 13 to col. 3, line 19).

In regards to claim 18, Komori further discloses an electronic apparatus (a semiconductor device of portable apparatus) provided with the semiconductor device defined in any one of claims 1-12 (col. 1, line 13 to col. 3, line 19).

3. Applicant's arguments filed 5/11/04 have been fully considered but they are not persuasive.

It is urged, in pages 7-9 of the remarks, that Komori never discloses or suggests the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layer levels, respectively. However, figs. 40 and 41 of Komori show the first drain-gate wiring layer [111] and the second drain-gate wiring layer [116] are located in different layer levels, respectively. The first drain-gate wiring layer [111] is formed on the insulating layer [2] while the second drain-gate wiring layer [116] is formed on the insulating film [300]. The insulating layer [2] and the insulating film [300] are located at different layer levels. Komori shows all the elements of the claimed invention as claimed in claims 1-12, 17 and 18.

4. Claims 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: The major difference in the claims not found in the prior art of record is the first

drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in a second conductive layer level.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl  
July 2, 2004

Steven Loke  
Primary Examiner

